Claim Amendments

1-27. (Canceled)

28. (Currently Amended) A processor, comprising:

multiple programmable ~~engines~~ units integrated within the processor; and

circuitry integrated within the processor to map resources within the multiple ~~engines~~ programmable units into a single address space, the circuitry to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second processor specifying an address within the single address space, wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units.

29. (Currently Amended) The processor of claim 28, wherein the resources within the multiple programmable ~~engines~~ units comprise ~~registers~~ register locations within the multiple programmable ~~engines~~ units.

30. (Currently Amended) The processor of claim 28, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable ~~engines~~ units.

31. (Currently Amended) The processor of claim 30, wherein the shared resources external to the multiple programmable ~~engines~~ units comprise ~~at least one of:~~ a memory internal to the processor, a randomly accessible memory external to the processor, and a Peripheral Component Interconnect (PCI) unit.

32. (Currently Amended) The processor of claim 28, wherein the multiple programmable ~~engines~~ units comprise multiple programmable multi-threaded ~~engines~~ units.

33. (Original) The processor of claim 28, further comprising an interface to a media access controller (MAC).

34. (Currently Amended) The processor of claim 28, wherein the circuitry comprises circuitry to receive a command from a programmable processor ~~other than the multiple programmable engines~~.

35. (Currently Amended) The semiconductor chip of claim 34, wherein the ~~programmable processor other than the multiple programmable engines comprises a programmable processor integrated within the processor~~ the multiple programmable units comprise multiple programmable engines and the programmable processor.

36. (Currently Amended) A method, comprising:

mapping ~~an address~~ addresses in a single address space to ~~a resource~~ resources within ~~one of~~ a set of multiple programmable ~~engines~~ units integrated within a processor, the single address space including addresses for different ones of the resources in different ones of the multiple programmable ~~engines~~ units; and

providing data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second processor specifying an address within the single address space, wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units

37. (Original) The method of claim 36, further comprising receiving a command specifying the address in the single address space.

38. (Original) The method of claim 37, wherein the command comprises one of: a read command and a write command.

39. (Currently Amended) The method of claim 37, wherein the receiving the command comprises receiving the command from a programmable processor ~~other than one of the multiple programmable engines~~.

40. (Currently Amended) The method of claim 39, wherein the programmable processor comprises a programmable processor integrated within the processor; and

wherein the multiple programmable units comprise multiple programmable engines and the programmable processor.

41. (Currently Amended) The method of claim 36, wherein the ~~resource~~ resources within ~~the one of~~ the set of multiple programmable ~~engines~~ units comprises ~~at least one~~ register locations within the multiple programmable units.

42. (Currently Amended) The method of claim 36, wherein the single address space comprises addresses corresponding to shared resources external to the multiple programmable ~~engines~~ units.

43. (Currently Amended) The method of claim 36, wherein the multiple programmable ~~engines~~ units comprise multiple programmable multi-threaded engines.

44. (Currently Amended) A device, comprising:

at least one Ethernet media access controller (MAC); and

at least one processor coupled to the at least one Ethernet media access controller, the processor comprising:

multiple programmable ~~multi-threaded engines~~ units;and

circuitry to map resources within the multiple programmable ~~engines~~ units and resources external to the multiple programmable ~~engines~~ units into a single address space, the resources within the multiple programmable ~~engines~~ units comprising ~~registers~~ register locations, the resources external to the multiple engines comprising at least one Random Access Memory (RAM) external to the processor, the circuitry to provide data access to a resource within a first of the multiple programmable units to a second one of the multiple programmable units in response to a data access request of the second processor specifying an address within the single address space, wherein there is a one-to-one correspondence between respective addresses in the single address space and respective resources within the multiple programmable units.

45. (Currently Amended) The device of claim 44, wherein the ~~processor further comprises~~ multiple programmable units comprise multiple programmable engines and a programmable processor integrated within the processor, the programmable processor having a different architecture than the multiple programmable engines.